WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer for silicide on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer for silicide;

thermally treating the Ni-based metal layer for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer for silicide and the N-rich titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed.

2. The method as claimed in claim 1, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

3. The method as claimed in claim 1, wherein the Ni-based metal layer for silicide is nickel or a nickel alloy.

4. The method as claimed in claim 1, wherein the Ni-based metal layer for silicide is a nickel layer including 0 to about 20 at% of one of Ta, Zr, Ti, Hf, W, Co, Pt, Pd, V, Nb, or any combination thereof.

5. The method as claimed in claim 1, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

6. The method as claimed in claim 1, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

7. The method as claimed in claim 1, further comprises etching the silicon substrate using an RF sputter etching process to remove particles from the substrate after forming the source/drain region.

8. The method as claimed in claim 7, wherein the RF sputter etching process comprises forming the Ni-based metal layer for silicide and the N-rich titanium nitride layer in-situ.

9. A semiconductor device which comprises:

a gate pattern and source/drain region formed on a silicon substrate;

a Ni-based metal layer for silicide formed on the silicon substrate by depositing Nickel or a Nickel alloy on an entire surface of the silicon substrate;

an N-rich titanium nitride layer formed on the Ni-based metal layer for silicide; and

a Nickel silicide layer formed on the gate pattern and the source/drain regions by thermally treating the Ni-based metal layer for silicide and the N-rich titanium nitride layer, and wherein the Ni-based metal layer for silicide and the N-rich titanium nitride layer are selectively removed such that a top portion of the nickel silicide layer on the gate pattern and the source/drain region are exposed.

10. The semiconductor device of claim 9, wherein the N-rich titanium nitride layer formed on the Ni-based metal layer for silicide is formed by loading the silicon substrate including the Ni-based metal layer for silicide into a chamber, and then injecting a nitrogen gas and a titanium source gas into the chamber.

11. The semiconductor device of claim 9, wherein the the Ni-based metal layer for silicide and the N-rich titanium nitride layer are selectively removed by performing a wet cleaning process.

12. A method for fabricating a semiconductor device comprising:

forming a field region on a substrate to define an active region;

forming a gate pattern on the active region, wherein the gate pattern includes sidewalls;

forming spacers on the sidewalls of the gate pattern;

forming source/drain regions aligned with the spacers on both sides of the gate pattern;

cleaning the substrate using a wet cleaning process;

forming a Ni-based metal layer for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer on the Ni-based metal layer;

thermally treating the Ni-based metal layer for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

cleaning the substrate to selectively remove the Ni-based metal layer for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region.

13. The method as claimed in claim 12, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

14. The method as claimed in claim 12, wherein the Ni-based metal layer for silicide is nickel or a nickel alloy.

15. The method as claimed in claim 12, wherein the Ni-based metal layer for silicide is a nickel layer including 0 to about 20 at% of one of Ta, Zr, Ti, Hf, W, Co, Pt, Pd, V, Nb, or any combination thereof.

16. The method as claimed in claim 12, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

17. The method as claimed in claim 12, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

18. The method as claimed in claim 12, further comprises etching the silicon substrate using an RF sputter etching process to remove particles from the substrate after forming the source/drain region.